

ABSTRACT OF THE INVENTION

5 A switch fabric implemented on a chip includes an array
of cells and an I/O interface in communication with the
array of cells for permitting exchange of data packets
between said array of cells and components external to
said array of cells. Each cell communicates with at
least one other cell of the array, thereby permitting an
exchange of data packets to take place between the cells
10 of the array. Each cell includes a memory for receiving
a data packet from another cell of the array as well as a
control entity to control release of a data packet toward
a selected destination cell of the array at least in part
on a basis of a degree of occupancy of the memory in the
15 destination cell. In this way, scheduling is distributed
amongst the cells of the switch fabric.

09870800-060101